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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>		Application Number	09/412,512
		Filing Date	October 5, 1999
		First Named Inventor	Shunpei YAMAZAKI
		Group Art Unit	2812
		Examiner Name	R. Booth
Sheet: 1	of 1	Attorney Docket Number	0756-2046

U.S. PATENT DOCUMENTS						
Examiner Initials ¹	Cite No. ¹	U.S. Patent Document		Name of Person or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Examiner Initials ¹	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	† ³
		J. Jang, et al., "32.1: Invited Paper: a-Si TFTs With Planarized Gate Insulators," Society for Information Display International Symposium Digest of Technical Papers, Volume XXX, San Jose Convention Center, San Jose, California, May 18-20, 1999, pp. 728-731.	

Examiner Signature	<i>Richard A. H.</i>	Date Considered	12/1/03
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